	Embedded System Design	Semester	06
Course Code	BEC601	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	
Examination nature (SEE)	Theory		

Course objectives:

- Identify various components, their purpose, and their application to the embedded system's applicability.
- Program various embedded components using the embedded C program.
- Understand the embedded system's real-time operating system and its application in IoT
- Understand the fundamentals of ARM-based systems, including architecture and its units like registers , debug interface, stack, MPU, Interrupts etc
- Use the various instructions to program the ARM controller.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. In addition to the traditional lecture method, different types of innovative teaching methods may be adopted so that the delivered lessons shall develop students' theoretical and applied Mathematical skills.
2. Provide real-life examples.
3. Support and guide the students for self–study.
4. You will assign homework, grading assignments and quizzes, and documenting students' progress.
5. Encourage the students to group learning to improve their creative and analytical skills.
6. Show short related video lectures in the following ways:
   - As an introduction to new topics (pre-lecture activity).
   - As a revision of topics (post-lecture activity).
   - As additional examples (post-lecture activity).
   - As an additional material of challenging topics (pre-and post-lecture activity).
   - As a model solution of some exercises (post-lecture activity).

MODULE-1

Introduction to Embedded System: What is an Embedded Systems? Embedded systems Vs General computing systems, History of Embedded Systems, Classification of Embedded systems, Major Application Areas of Embedded Systems. Purpose of Embedded Systems, The Typical Embedded System, Microprocessor Vs Microcontroller, Differences between RISC and CISC, Harvard V/s Von-Neumann Processor/Controller Architecture, Big-endian V/s Little-endian processors, Memory (ROM and RAM types), Sensors & Actuators, The I/O Subsystem – I/O Devices, Light Emitting Diode (LED), 7-Segment LED Display, Optocoupler, Relay, Piezo buzzer, Push button switch, Communication Interfaces, On-board Communication Interface, External Communication Interface, Embedded Firmware, Other System Components

(Text 1: All the Topics from Ch-1 and Ch-2.)

MODULE-2

Embedded System Design Concepts: Characteristics and Quality Attributes of Embedded Systems, Operational and non-operational quality attributes, Embedded Systems-Application and Domain specific, Hardware Software Co-Design and Program Modeling (excluding UML), Embedded firmware design and development (excluding C language).

Text 1: Ch-3, Ch-4 (4.1, 4.2.1 and 4.2.2 only), Ch-7 (Sections 7.1, 7.2 only), Ch-9 (Sections 9.1, 9.2, 9.3.1, 9.3.2 only)
MODULE-3
RTOS and IDE for Embedded System Design: Operating System basics, Types of operating systems, Task, process and threads (Only POSIX Threads with an example program), Thread preemption, Preemptive Task scheduling techniques, Task Communication, Task synchronization issues – Racing and Deadlock. How to choose an RTOS, Integration and testing of Embedded hardware and firmware, Embedded system Development Environment – Block diagram (excluding Keil). **(Text 1: Ch-10 (Sections 10.1, 10.2, 10.3, 10.5.2 , 10.7, 10.8.1.1, 10.8.1.2 only), Ch-12, Ch-13 (a block diagram before 13.1, only).**
MODULE-4
ARM Embedded Systems: Introduction, RISC design philosophy, ARM design philosophy, Embedded system hardware – AMBA bus protocol, ARM bus technology, Memory, Peripherals, Embedded system software – Initialization (BOOT) code, Operating System, Applications. ARM Processor Fundamentals, ARM core dataflow model, registers, current program status register, Pipeline, Exceptions, Interrupts and Vector Table, Core extensions. **Text 2: Chapter 1, 2**
MODULE-5
Introduction to the ARM Instruction set: Introduction, Data processing instructions, Load – Store instruction, Software interrupt instructions, Program status register instructions, Loading constants, ARMv5E extensions, Conditional Execution. **Text 2: Chapter 3**

PRACTICAL COMPONENT OF IPCC

Conduct the following experiments on an ARM CORTEX M3 evaluation board to learn Assembly Language Program and using evaluation version of Embedded 'C' & Keil uVision-4 tool/compiler.

Sl.NO	Experiments
1	Write a program to find the sum of the first 10 integer numbers.
2	Write an Assembly Language Program (ALP) to i) Multiply two 16-bit numbers. ii) Add two 32-bit numbers.
3	Write a program to find the factorial of a number.
4	Write a program to add an array of 16 bit numbers and store the 32 bit result in internal RAM.
5	Write a program to find the square of a number (1 to 10) using a look-up table.
6	Write a program to find the largest or smallest number in an array of 32 numbers.
7	Write a program to arrange a series of 32 bit numbers in ascending/descending order.
8	Write a program to count the number of ones and zeros in two consecutive memory locations.
9	Interface a Stepper motor and rotate it in clockwise and anti-clockwise direction.
10	Interface a DAC and generate Triangular and Square waveforms.
11	Display the Hex digits 0 to F on a 7-segment LED interface, with a suitable delay in between.
12	Interface a simple Switch and display its status through Relay, Buzzer and LED

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Describe the architectural features and instructions of 32-bit microcontroller ARM Cortex M3.
- Apply the knowledge gained for Programming ARM Cortex M3 for different applications.
- Understand the basic hardware components and their selection method based on the characteristics and attributes of an embedded system.
- Understand the hardware software co-design and firmware design approaches.
- Explain the need of real time operating system for embedded system applications.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

CIE for the theory component of the IPCC (maximum marks 50)

- IPCC means practical portion integrated with the theory of the course.
- CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.
- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.
- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

Suggested Learning Resources:

Text Books

1. **Shibu K V, "Introduction to Embedded Systems", Tata McGraw Hill Education**
2. **Andrew N Sloss, Dominic System and Chris Wright, "ARM System Developers Guide", Elsevier, Morgan Kaufman publisher, 1st Edition, 2008.**

Reference Book

1. **Raj Kamal, "Embedded Systems: Architecture and Programming", Tata McGraw Hill, 2008.**

Web links and Video Lectures (e-Resources):

1. https://archive.nptel.ac.in/courses/106/105/106105193/
2. https://developer.arm.com/documentation/dui0068/b/ARM-Instruction-Reference
3. https://www.udemy.com/course/introduction-to-arm-cortex-m3-and-m4-processors/
4. www.Nuvoton .com/websites on Advanced ARM Cortex Processors
5. https://alison.com/tag/embedded-systems

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Programming Assignments / Mini Projects can be given to improve programming skills

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	VLSI Design and Testing	Semester	5
Course Code	**BEC602**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		

Course objectives:

1.This course deals with analysis and design of digital CMOS integrated circuits.

2. The course emphasizes on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.

3. This course will also cover switching characteristics of digital circuits along with delay and power estimation.

4. Understanding the CMOS sequential circuits and memory design concepts.

5.Explore the knowledge of VLSI Design flow and Testing

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

MODULE-1

Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.

[Text 1: 1.1,1.2,1.3,1.4,1.5.1.6.]

Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2

MODULE-2

MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.

[Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

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Teaching-Learning Process:
Chalk and talk method/Power point presentation RBT Level: L1, L2, L3.

MODULE-3

CMOS Process Technology: Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. [Text 1: 3.1,3.2,3.3.]

Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield.
[Text 1: 4.1,4.2,4.3,4.4,4.5.4.6.4.7,4.8,4.9,4.10]

Teaching-Learning Process:
Chalk and talk method/Power point presentation, YouTube Videos RBT Level: L1, L2, L3.

MODULE-4

CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads.

[Text 1: 5.1,5.2,5.2.1, , 5.2.2, 5.2.3, 5.2.4, 5.2.6, 5.2.8, 5.3,5.3.1,5.3.2, 5.3.4 ,5.3.8,5.5]

Teaching-Learning Process:
Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3.

MODULE-5

Sequential MOS Logic Circuits: Introduction, Behaviour of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch.
[Text2: 8.1, 8.2, 8.3, 8.4]

Structured Design and Testing: Introduction**,** Design Styles, Testing
[Text1: 6.1, 6.2. 6.5]

Teaching-Learning Process:
Chalk and talk method/Power point presentation RBT Level: L1, L2, L3

Text Books:

1. Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company.
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.

Reference Books:

1. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.
2. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005.

Course Outcomes: After completing the course, the students will be able to

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CO1	Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors
CO2	Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.
CO3	Analyze the synchronous timing metrics for sequential designs and structured design basics.
CO4	Understand designing digital blocks with design constraints such as propagation delay and dynamic power dissipation.
C05	Understand the concepts of Sequential circuits design and VLSI testing

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	Multimedia Communication		Semester	6
	Course Code	**BCE613A**	CIE Marks	50
	Teaching Hours/Week (L:T:P: S)	3:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	
	Examination type (SEE)	Theory		

Course objectives:

- Gain fundamental knowledge in understanding the basics of different multimedia Networks and applications.
- Understand digitization principle techniques required to analyze different media Types.
- Analyze compression techniques required to compress text and image and gain Knowledge of DMS.
- Analyze compression techniques required to compress audio and video.
- Gain fundamental knowledge about multimedia communication across different Networks.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class.
4. Ask at least three HOTS(Higher-order Thinking)questions in the class, which promotes critical thinking
5. Topics will be introduced in multiple representations.
6. Discuss how every concept can be applied to the real world-and when that's possible, it helps improve the students' understanding.

Module-1

Multimedia Communications: Introduction, Multimedia information representation, Multimedia networks, multimedia applications, Application and networking terminology. (Chapter 1 of Text1)

Module-2

Information Representation: Introduction, Digitization principles, Text, Images, Audio and Video. (Chapter 2 of Text 1

Module-3

Text and Image Compression: Introduction, Compression principles, text compression, image Compression. (Chapter 3 of Text 1)

Module-4

Audio and video compression: Introduction, Audio compression, video compression, video compression principles, video compression. (Chapter 4 of Text 1)

Module-5

Multimedia Information Networks: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI (Chapter 8.1 to8.6of Text 1).

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Understand the basics of multimedia Communication and applications
2. Analyze media types to represent them in digital form.
3. Apply the compression techniques on text, images, audio and video.
4. Understand multimedia information networks.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks

Suggested Learning Resources:

Textbooks:

Multimedia Communications –Fred Halsall, Pearson Education,2001,ISBN-978813170994

ReferenceBooks:

1. Multimedia: Computing, Communications and Applications- Raif Steinmetz, Klara Nahrstedt, Pearson Education, 2002, ISBN-978817758
2. FundamentalsofMultimedia–Ze-NianLi,MarkSDrew,andJiangchuanLiu.

Web links and Video Lectures (e-Resources):

- Implementation of compression algorithms using MATLAB/any open source tools (Python, Scilab, etc.)

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- https://www.slideshare.net
  NPTEL Video Lectures
- https://archive.nptel.ac.in/courses/117/105/117105083/
- Multimedia Computing lecture: Communications & Networking –You Tube

B. E. (EC / TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VI

Data Security

Course Code	**BEC613B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory	Total Marks	100
CREDITS - 03			

Course objectives:

This course will enable students to:

- Preparation: To prepare students with fundamental knowledge/ overview in the field of Information Security with knowledge of mathematical concepts required for cryptography.
- Core Competence: To equip students with a basic foundation of Cryptography by delivering the basics of symmetric key and public key cryptography, authentication functions like HASH codes, MACs, digital signatures, as well as key distribution

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps to improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.
10. Give Programming Assignments.

MODULE-1	RBTL Level
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques (excluding Hill cipher) (Text 1: Chapter 1: Section 1, 2) **Block Ciphers**: Traditional Block Cipher structure, (Text 1: Chapter 2: Section1) The AES Cipher. (Text 1: Chapter 4: Section 2,4) Block Cipher Modes of Operation (Text 1: Chapter 5: Section 2, 3, 4, 5, 6)	L1, L2, L3
MODULE-2	
Basic Concepts of Number Theory and Finite Fields: Divisibility and The Division Algorithm Euclidean algorithm, Modular arithmetic, Groups, Rings and Fields, Finite fields of the form GF(p), Polynomial Arithmetic, Fields of the Form GF(2_m) (Text 1: Chapter 3)	L1, L2, L3
MODULE-3	

More on Number Theory: Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. (Text 1: Chapter 7: Section 1, 2, 5) **ASYMMETRIC CIPHERS**: Principles of Public-Key Cryptosystems, The RSA algorithm (Text 1: Chapter 8: Section 1, 2), Diffie – Hellman Key Exchange, Elliptic Curve Arithmetic over Z_p, Elliptic Curve Cryptography (Text 1: Chapter 9: Section 1, 3, 4)	L1, L2, L3
MODULE-4	
Cryptographic Hash Functions: Application of Hash Functions, Two Simple Hash Functions, Requirements and Security, Hash function based on Cipher Block Chaining, SHA-512 (Only structural description). (Text 1: Chapter 10: Section 1, 2, 3, 4, 5) **Message Authentication Codes:** Message Authentication Functions, Security of MACs, MACs based on Hash Functions. (Text 1: Chapter 11: Section 2, 4, 5)	L1, L2, L3
MODULE-5	
Digital Signatures: Digital Signatures, NIST Digital Signature Algorithm, Elliptic Curve Digital Signature Algorithm. (Text 1: Chapter 12: Section 1, 4, 5) **Key Management and Distribution:** Symmetric Key Distribution Using Symmetric Encryption, Symmetric Key Distribution Using Asymmetric Encryption, Distribution of Public Keys (Text 1: Chapter 13: Section 1, 2, 3)	L1, L2, L3

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain traditional cryptographic algorithms of encryption and decryption process.
- Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the data.
- Apply concepts of modern algebra in cryptography algorithms.
- Explain message authentication using HASH functions, MAC functions and Digital signatures.
- Explain how symmetric and asymmetric encryption algorithms can be used to distribute keys.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks.
- Any two assignment methods mentioned in the 22OB4.2, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks).
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:
Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Text Book

1. William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3

Reference Books

1. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.
2. Cryptography and Network Security, Behrouz A Forouzan, TMH, 2007.

Web links and Video Lectures (e-Resources):

- https://archive.nptel.ac.in/courses/106/105/106105162

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

1. Experiential Learning by using free and open-source software's SCILAB or OCTAVE or Python

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI

B.E: Electronics & Communication Engineering / B.E: Electronics & Telecommunication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2021 – 22)

VI Semester

Digital Image Processing			
Course Code	**BEC613C**	CIE Marks	50
Teaching Hours/Week (L:T:P:S)	3:0:0:1	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	3	Exam Hours	3

Course objectives:

- Understand the fundamentals of digital image processing.
- Understand the image transform used in digital image processing.
- Understand the image enhancement techniques in spatial domain used in digital image processing.
- Understand the Color Image Processing and frequency domain enhancement techniques in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Show Video/animation films to explain the functioning of various image processing concepts.
2. Encourage cooperative (Group) Learning through puzzles, diagrams, coding etc., in the class.
3. Encourage students to ask questions and investigate their own ideas helps improve their problem-solving skills as well as gain a deeper understanding of academic concepts.
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Students are encouraged to do coding based projects to gain knowledge in image processing.
6. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
7. Topics will be introduced in multiple representations.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding
9. Arrange visits to nearby PSUs such as CAIR (DRDO), NAL, BEL, ISRO, etc., and small-scale software industries to give industry exposure.

Module-1

Digital Image Fundamentals: What is Digital Image Processing? Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships Between Pixels.
[Text 1: Chapter 1, Chapter 2: Sections 2.1 to 2.5]

Teaching-Learning Process	Chalk and talk method, PowerPoint Presentation, YouTube videos, Videos on Image processing applications Self-study topics: Arithmetic and Logical operations Practical topics: Problems on Basic Relationships Between Pixels. **RBT Level:** L1, L2, L3

<table>
<tr><th colspan="2">Module-2</th></tr>
<tr><td colspan="2">Image Transforms: Introduction, Two-Dimensional Orthogonal and Unitary Transforms, Properties of Unitary Transforms, Two-Dimensional DFT, cosine Transform, Haar Transform.
Text 2: Chapter 5: Sections 5.1 to 5.3, 5.5, 5.6, 5.9]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos of various transformation techniques and related applications.
Self-study topics: Sine transforms, Hadamard transforms, KL transform, Slant transform.
Practical topics: Problems on DFT and DCT
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-3</th></tr>
<tr><td colspan="2">Spatial Domain: Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters
[Text: Chapter 3: Sections 3.2 to 3.6]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos and animations of Intensity Transformation Functions, Histogram Processing, Spatial domain filters.
Self-study topics: Point, line and edge detection.
Practical topics: Problems on Intensity Transformation Functions, Histogram, Spatial domain filters
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-4</th></tr>
<tr><td colspan="2">Frequency Domain: Basics of Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters.
Color Image Processing: Color Fundamentals, Color Models, Pseudo-color Image Processing.
[Text 1: Chapter 4: Sections 4.7 to 4.9 and Chapter 6: Sections 6.1 to 6.3]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos on frequency domain filtering, Color image processing.
Self-study topics: Basic concept of segmentation.
Practical topics: Problems on Pseudo-color Image Processing
RBT Level: L1, L2, L3</td></tr>
<tr><th colspan="2">Module-5</th></tr>
<tr><td colspan="2">Restoration: A model of the Image Degradation/Restoration Process, Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering.
[Text 1: Chapter 5: Sections 5.1, to 5.4.3, 5.7, 5.8]</td></tr>
<tr><td>Teaching-Learning Process</td><td>Chalk and talk method, PowerPoint Presentation, YouTube videos on Noise models, filters and their applications.
Self-study topics: Linear position invariant degradation, Estimation of degradation function.
RBT Level: L1, L2, L3</td></tr>
<tr><td colspan="2">Course outcomes (Course Skill Set)
At the end of the course the student will be able to:
1. Understand image formation and the role of human visual system plays in the perception of gray andcolor image data.
2. Compute various transforms on digital images.
3. Conduct an independent study and analysis of Image Enhancement techniques.
4. Apply image processing techniques in the frequency (Fourier) domain.
5. Design image restoration techniques.</td></tr>
</table>

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. Digital Image Processing- Rafael C Gonzalez and Richard E Woods, PHI, 3rd Edition 2010.
2. Fundamentals of Digital Image Processing- A K Jain, PHI Learning Private Limited 2014.

Reference Book:

Digital Image Processing- S Jayaraman, S Esakkirajan, T Veerakumar, Tata McGraw Hill, 2014.

Web links and Video Lectures (e-Resources)

- Image databases, https://imageprocessingplace.com/root_files_V3/image_databases.htm
- Student support materials, https://imageprocessingplace.com/root_files_V3/students/students.htm
- NPTEL Course, Introduction to Digital Image Processing, https://nptel.ac.in/courses/117105079
- Computer Vision and Image Processing, https://nptel.ac.in/courses/108103174
- Image Processing and Computer Vision – Matlab and Simulink,
- https://in.mathworks.com/solutions/image-video-processing.html

Activity Based Learning (Suggested Activities in Class)/ Practical Based Learning

- Verilog /VHDL coding for Image manipulation.
- Simulink models for Image processing.

FPGA Based System design Using Verilog		Semester	VI
Course Code	BEC613D	CIE Marks	50
Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	03
Examination type (SEE)	THEORY		

Course objectives:

This course will enable students to:

- Understand the types programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx FPGAs.
- Understand the concepts of Advanced Logic design and implementation using Verilog HDL
- Designing different Digital applications using SM chart .

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

These are sample Strategies, which teachers can use to accelerate the attainment of the various courseoutcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different types of teaching methods may be adopted to develop the outcomes.
2. Encourage collaborative (Group) Learning in the class.
3. Ask at least three HOTS (Higher Order Thinking) questions in the class, which promotes criticalthinking.
4. Adopt Problem-Based Learning (PBL), which fosters students' Analytical skills, and develops thinking skillssuch as the ability to evaluate, generalize, and analyze information rather than simply recall it.
5. Topics will be introduced in a multiple representation.
6. Show the different ways to solve the same problem and encourage the students to come up withcreative ways to solve them.
7. Discuss how every concept can be applied to the real world and when that's possible, it helps improve the student's understanding.
8. Adopt the Flipped class technique by sharing the materials/Sample Videos before the class and having discussions on the topic in the succeeding classes.

Module-1

Introduction to Programmable Logic Devices:

Hazards in Combinational Circuits, Brief overview of Programmable Logic Devices, Simple Programmable Logic Devices (SPLDs)
Complex Programmable Logic devices (CPLDs), Field-Programmable Gate Arrays (FPGAs)

(Text 1: 1.5,3.1,3.2 , 3.3, 3.4) RBT Level: L1, L2, L3

Module-2

Advanced Digital Design Examples:
BCD to 7-Segment Display Decoder, BCD Adder, Traffic Light controller, Synchronization and debouncing, Shift-and-Add Multiplier
Array Multiplier, A Signed Integer/Fraction Multiplier, (Excluding Test Bench) , Keypad Scanner (Excluding Test Bench)

Module-3

SM Charts and Microprogramming :
State Machine Charts, Derivation of SM Charts, SM chart for binary multiplier , Dice Game (Excluding Test Bench) , Realization of SM Charts , Implementation of the Dice Game . Microprogramming , Linked State Machines.
(**Text 1: 5.1, 5.2, 5.3 , 5.4 , 5.5 , 5.6) RBT Level:** L1, L2, L3

Module-4

Floating-Point Arithmetic: Representation of Floating-Point Numbers, Floating-Point Multiplication, Floating-Point Addition, Other Floating-Point Operations.
Multivalued Logic and Signal Resolution, Built-in Primitives, User-Defined Primitives, SRAM Model, Rise and Fall Delays of Gates, Rise and Fall Delays of Gates

(Text 1:7.1,7.2, 7.3,7.4, 8.3, 8.4, 8.5,8.6,8.8) RBT Level: L1, L2, L3

Module-5

Designing with Field Programmable Gate Arrays :
Implementing Functions in FPGAs, Implementing Functions Using Shannon's Decomposition Carry Chains in FPGAs , Cascade Chains in FPGAs , Examples of Logic Blocks in Commercial FPGAs , Examples of Logic Blocks in Commercial FPGAs, Dedicated Multipliers in FPGAs, FPGAs Capacity: Maximum gates versus Usable gates , Design Translation.

(Text 1: 6.1,6.2,6.3, 6.4 ,6.5 , 6.6, 6.7, 6.8,6.10, 6.11) RBT Level: L1, L2, L3

Course outcome (Course Skill Set)

At the end of the course the student will be able to:

1. Apply the concept of Programmable logic devices to implement digital design.
2. Design and implementation of Advanced logic design using Verilog HDL
3. Understand the concept of SM Chart and design complex digital circuits using SM Chart.
4. Performing the Floating-point arithmetic operations and designing of Memories
5. Designing and performance evaluation of advanced digital design using FPGAs

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.

Suggested Learning Resources:

Text Book:

1 Digital Systems Design Using Verilog First Edition, Charles H. Roth, Jr. The University of Texas at Austin, Lizy Kurian John The University of Texas at Austin, Byeong Kil Lee The University of Texas at San Antonio

Reference Books:

1. Advanced FPGA Design Architecture, Implementation, and Optimization Steve Kilts Spectrum

2. ASIC and FPGA Verification: A guide to component Modelling.
Richard Munden, Morgan Kaufmann Publishers is an imprint of Elsevier

3. Processor Design . System-on-Chip Computing for ASICs and FPGAs, Jari Nurmi Finland Tampere University of Technology Sringer Publications.

4. The design Warrior's guide to FPGA Clive 'Max' Maxfield Elsevier Publications

Activity Based Learning (Suggested Activities in Class)/Practical-Based Learning

- Group Discussion/Quiz
- Demonstration of Verilog and FPGA concepts.
- Case Study on small design and implementation on FPGA's

Digital System Design using Verilog		Semester	6
Course Code	**BEC654A**	CIE Marks	50
Teaching Hours/Week(L:T:P)	3:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3
Examination type (SEE)	Theory		

Course objectives:

- Learn different Verilog HDL constructs.
- Familiarize the different levels of abstraction in Verilog.
- Understand Verilog Tasks and Functions.
- Understand Timing and Delay Simulation.

Teaching-Learning Process (General Instructions)

The sample strategies, which the teacher can use to accelerate the attainment of the various course outcomes are listed in the following:

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various techniques.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
8. Give programming assignments.

Module-1

Overview of Digital Design with Verilog HDL: Evolution of Computer-Aided Digital Design (CAD), Emergence of HDLs, Typical Design flow, Importance of HDLs, Popularity of Verilog HDL, Trends in HDLs. (**Text 1: 1.1 to 1.6**)

Hierarchical Modeling Concepts: Design Methodologies, Top-down and Bottom-up design methodology, Modules, Instances, Components of a Simulation, Design Block, Stimulus Block (Test Bench) with example. **(Text 1:2.1 to 2.6)**

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-2

Basic Concepts: Lexical Conventions, Data Types, System Tasks, Compiler Directives. **(Text 1: 3.1 to 3.3)**

Modules and Ports: Modules, Ports, Connecting Ports, Hierarchical Names. **(Text 1: 4.1 to 4.3)**

Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3

Module-3	
Gate-Level Modeling: Gate Types-Modeling using basic Verilog gate primitives, Description of AND/OR and BUF/NOT type gates. Gate Delays-Rise, Fall and Turn-Off Delays, Min, Max and Typical Delays. **(Text1: 5.1, 5.2)** **Dataflow Modeling**: Continuous assignments, Delay Specification, Expressions, Operators, Operands, Operator Types, Examples **(Text 1: 6.1 to 6.5)**	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-4	
Behavioral Description: Structured Procedures, Initial and Always statements, Procedural Assignments Blocking and Non-Blocking statements, Conditional statements, Multiway Branching, Loops, Sequential and Parallel blocks, Examples-4-to-1 Multiplexer, 4-bit Counter. **(Text 1: 7.1, 7.2, 7.4, 7.5, 7.6, 7.7, 7.9.1, 7.9.2)**	
Teaching-Learning Process	Chalk and talk method, Power point presentation **RBT Level:** L1, L2, L3
Module-5	
Structural Description: Highlights of Structural Descriptions, Organization of Structural Description, Binding **(Text 2: 4.1, 4.2, 4.3, Listings 4.1 to 4.13 only Verilog)** **Tasks and Functions**: Differences between Tasks and Functions, Declaration and Invocation, Examples **(Text 1: 8.1, 8.2, 8.2.1, 8.2.2, 8.3, 8.3.1, 8.3.2)**	

Course outcomes (Course Skill Set)

At the end of the course the student will be able to:

1. Understand the Verilog HDL design flow.
2. Describe the basic concepts of Verilog HDL programming.
3. Write Verilog programs in Gate, Dataflow, Behavioral, and structural modeling levels of Abstraction.
4. Write the programs more effectively using Verilog Tasks and Functions.
5. Perform Timing and Delay Simulation.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures not less than 35% (18 Marks out of 50) in the semester-end examination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

Three Unit Tests each of **20 Marks (duration 01 hour**)

1. First test at the end of 5th week of the semester
2. Second test at the end of the 10th week of the semester
3. Third test at the end of the 15th week of the semester

Two assignments each of **10 Marks**

4. First assignment at the end of 4th week of the semester
5. Second assignment at the end of 9th week of the semester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20 Marks** (**duration 01 hours**)

6. At the end of the 13th week of the semester

The sum of three tests, two assignments, and quiz/seminar/group discussion will be out of 100 marks and will be **scaled down to 50 marks**

(to have less stressed CIE, the portion of the syllabus should not be common /repeated for any of the methods of the CIE. Each method of CIE should have a different syllabus portion of the course).

CIE methods /question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the subject (**duration 03 hours)**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.

The students have to answer 5 full questions, selecting one full question from each module. Marks scored out of 100 shall be reduced proportionally to 50 marks

Suggested Learning Resources:

Text Books:

1. "Verilog HDL: A Guide to Digital Design and Synthesis", Samir Palnitkar, Pearson education, Second edition.
2. "HDL programming (VHDL and Verilog)", Nazeih M Botros, John Wiley India Pvt. Ltd., 2008.

Reference Books:

1. Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science+Business Media, LLC, Fifth edition.
2. Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3. Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016 or earlier

	Consumer Electronics		Semester	6
	Course Code	**BEC654B**	CIE Marks	50
	Teaching Hours/Week (L: T:P: S)	3:0:0:0	SEE Marks	50
	Total Hours of Pedagogy	40	Total Marks	100
	Credits	03	Exam Hours	03
	Examination type (SEE)	Theory		

Course objectives:

- To understand the working principles and classifications of various microphones and loudspeakers, and their roles in audio systems.
- To explore the structure, recording, and playback processes of Audio Compact Disc systems, along with error correction techniques and digital-to-analog conversion.
- To analyse the fundamentals of colour television systems, including the transmission of colour signals, and to study recent advances in television technology.
- To gain knowledge of modern consumer electronic devices such as mobile phones, home appliances, and computers, focusing on their applications and technological advancements.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the functioning of various EV Architectures.
3. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
4. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Microphones: Introduction, Requirements, Quality of Microphones, Classification, Moving Coil Microphone, Ribbon Microphone, Condenser (or Capacitor) Microphone, Crystal Microphone, Carbon Microphone, Electret Microphone.

Loudspeakers: Introduction, Features of Loudspeaker, Moving Coil (Cone Type) Loudspeaker, Electrodynamic Loudspeaker, Horn Loudspeaker, Loudspeaker for High Fidelity Systems.

(Text : 5.1 to 5.10 and 6.1 to 6.6)

Module-2

Audio Compact Disc Systems: Introduction, Comparison of CD and Tape, Optical Recording, Details of a Compact Disc, Details of Recording Process, Details of playback Process, Geometry of Audio Disc, Encoding Process and Error Correction, D/A Convertor, Handling of Compact Disc.

(Text : 10.1 to 10.10)

Module-3

Colour Television: Introduction, Light Energy, Primary Colours, Tristimulus Values, Trichromatic Coefficients, Colour Triangle, Mixing of Colours, Grassman's Law, Colour Specifications, Bandwidth for Colour Signal Transmission. Chromaticity Diagram, Spectral and Non-Spectral Colours, Colour Circle, Visibility Curve, Digital Television (DTV) and High Definition Television (HDTV), Recent Advances in TV technology, LCD TV, LED TV, Plasma TV

(Text : 14.1 to 14.9, 14.13 to 14.16 and 14.26 to 14.27)

Module-4

	Cable Television: Introduction, Video Monitor, Closed Circuit Television (CCTV), Cable Television, Cable TV Using Internet. **Miscellaneous Devices:** Digital Watch, Calculator, An Electronic Guessing Game, Cordless Telephone. (Text : 15.1 to 15.5 and 17.1 to 17.4)
	Module-5
	Mobile Telephone, Cellular Telephone, UPS, Inverter, Decorative Lighting, Remote Control for TV and VCR, Facsimile (FAX), Pager, Microwave Oven, LCD Timer with Alarm, Electronic Ignition System for Automobiles, Washing Machine, Organisation of Digital computer, Microprocessor, Note Book, Laptop, Tablet PC, Ultrabook, IPAD, Recent Advances in Consumer Electronics. (Text : 17.6 to 17.7 and 17.13 to 17.27)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to:

1. Understand the functioning and classification of various types of microphones and loudspeakers
2. Demonstrate knowledge of the optical recording and playback processes in audio compact disc systems
3. Analyse the principles of colour television and modern display technologies
4. Evaluate the working of cable television systems and miscellaneous consumer devices
5. Explore advancements in consumer electronics, such as mobile phones, computing devices, and home appliances

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- For the Assignment component of the CIE, there are 25 marks and for the Internal Assessment Test component, there are 25 marks.
- The first test will be administered after 40-50% of the syllabus has been covered, and the second test will be administered after 85-90% of the syllabus has been covered
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The teacher should not conduct two assignments at the end of the semester if two assignments are planned.
- For the course, CIE marks will be based on a scaled-down sum of two tests and other methods of assessment.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. B.R. Gupta, V. Singhal "Consumer Electronics", S.K. Kataria & Sons, 6th edition, 2013, ISBN 978-93-5014-407-7.
2. R.P.Bali, Consumer Electronics, Pearson Education (2008)

Web links and Video Lectures (e-Resources):

- Android Mobile Application Development: https://onlinecourses.swayam2.ac.in/nou24_ge66/preview
- Microelectronics: Devices to Circuits: https://onlinecourses.nptel.ac.in/noc24_ee139/preview

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

- Trouble shoot the common consumer electronics products like T.V., Washing machine , microwave oven , FAX, Copier machine.
- Conduct market survey for latest home appliances and compare specifications of reputed brands and prepare a report
- Make visit to service centres of gadgets covered in curriculum and if possible work there for some days on voluntarily basis during holidays.
- Search internet websites for DYS (Do Your Self) repair of electronic gadgets and try your hands to repair some gadgets based on that.

Electronic Communication Systems		Semester	6
Course Code	BEC654C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:0:0	SEE Marks	50
Total Hours of Pedagogy	40	Total Marks	100
Credits	03	Exam Hours	3 Hours
Examination type (SEE)	**Theory**		

Course objectives:

- Describe essential elements of an electronic communication system.
- Understand Amplitude, Frequency & Phase modulations, and Amplitude demodulation.
- Define the sampling theorem and methods to generate pulse modulations.
- Learn the various methods of digital modulation techniques and compare the different schemes.
- Introduce the basic concepts of information theory and coding.
- Understand the basic concepts of wireless and cellular communications.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only the traditional lecture method, but a different type of teaching method may be adopted to develop the outcomes.
2. Show Video/animation films to explain the evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher-order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

Module-1

Introduction to Electronic Communications: Historical perspective, Electromagnetic frequency spectrum, Signal and its representation, Elements of electronic communications system, primary communication resources, signal transmission concepts, Analog and digital transmission, Modulation, Concept of frequency translation, Signal radiation and propagation (Text 1: 1.1 to 1.10)

Module-2

Amplitude Modulation Techniques: Types of analog modulation, Principle of amplitude modulation, AM power distribution, Limitations of AM, (TEXT 1: 4.1, 4.2, 4.4, 4.6)

Angle Modulation Techniques: Principles of Angle modulation, Theory of FM-basic Concepts, Theory of phase modulation (TEXT1: 5.1, 5.2, 5.5)

Module-3

Sampling Theorem and Pulse Modulation Techniques: Digital Versus Analog Transmissions, Sampling Theorem, Classification of pulse modulation techniques, PAM, PWM, PPM, PCM, Quantization of signals (TEXT 1: 7.2 to 7.8)

Module-4

Digital Modulation Techniques: Types of digital Modulation, ASK, FSK, PSK, QPSK. (TEXT 1: 9.1 to 9.5)

Information Theory, Source and Channel Coding: Information, Entropy and its properties, Shannon,- Hartley Theorem, Objectives of source coding, Source coding technique, Shannon source coding theorem, Channel coding theorem, Error Control and Coding. [Text1: 10.1,10.2, 10.11.2, 11.1 to 11.3, 11.8, 11.9, 11.12]

Module-5

Evolution of wireless communication systems: Brief History of wireless communications, Advantages of wireless communication, disadvantages of wireless communications, wireless network generations, Comparison of wireless systems, Evolution of next generation networks, Applications of wireless communication (TEXT 2: 1.1 to 1.7)

Principles of Cellular Communications: Cellular terminology, Cell structure and Cluster, Frequency reuse concept, Cluster size and system capacity, Method of locating cochannel cells, Frequency reuse distance (TEXT 2: 4.1 to 4.7)

Course outcome (Course Skill Set)

At the end of the course, the student will be able to :

1. Describe the scheme and concepts of radiation and propagation of communication signals through air.
2. Understand the AM and FM modulation techniques and represent the signal in time and frequency domain relations.
3. Understand the process of sampling and quantization of signals and describe different methods to generate digital signals.
4. Describe the basic digital modulation techniques, channel capacity, source coding technique and the channel coding.
5. Compare the different wireless communication systems and describe the structure of cellular communication.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation:

- There are 25 marks for the CIE's Assignment component and 25 for the Internal Assessment Test component.
- Each test shall be conducted for 25 marks. The first test will be administered after 40-50% of the coverage of the syllabus, and the second test will be administered after 85-90% of the coverage of the syllabus. The average of the two tests shall be scaled down to 25 marks
- Any two assignment methods mentioned in the 22OB2.4, if an assignment is project-based then only one assignment for the course shall be planned. The schedule for assignments shall be planned properly by the course teacher. The teacher should not conduct two assignments at the end of the semester if two assignments are planned. Each assignment shall be conducted for 25 marks. (If two assignments are conducted then the sum of the two assignments shall be scaled down to 25 marks)
- The final CIE marks of the course out of 50 will be the sum of the scale-down marks of tests and assignment/s marks.

Internal Assessment Test question paper is designed to attain the different levels of Bloom's taxonomy as per the outcome defined for the course.

Semester-End Examination:

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours).**

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored shall be proportionally reduced to 50 marks.

Suggested Learning Resources:

Books

1. T L Singal, Analog and Digital Communications, McGraw Hill Education (India) Private Limited, 2012, 0-07-107269-1.
2. 2. T L Singal, Wireless Communications, McGraw Hill Education (India) Private Limited, 2016, ISBN:0-07-068178-3.

Reference Books

1. Simon Haykin & Michael Moher, Communication Systems, 5th Edition, John Wiley, India Pvt. Ltd, 2010, ISBN: 978-81-265-2151-7.
2. Herbert Taub, Donald L Schilling, Goutam Saha, "Principles of Communication systems", 4th Edition, Mc Graw Hill Education (India) Private Limited, 2016. ISBN: 978-1-25-902985-1
3. Simon Haykin, "Digital Communication Systems", John Wiley & sons, 2014, ISBN 978-81- 265-4231-4

Web links and Video Lectures (e-Resources):
1. Communication Engineering **https://nptel.ac.in/courses/117102059**
Activity Based Learning (Suggested Activities in Class)/ Practical Based learning 1. Assignments and test – Knowledge level, Understand Level and Apply level 2. Experiential Learning by using free and open source software's SCILAB or OCTAVE or Python

VISVESVARAYATECHNOLOGICALUNIVERSITY,BELAGAVI
B.E:Electronics & Communication Engineering NEP, OutcomeBasedEducation (OBE)and ChoiceBased CreditSystem(CBCS)
(Effectivefromthe academicyear 2022–23)

VISemester

BasicVLSIDesign			
CourseCode	**21EC654D**	CIEMarks	50
TeachingHours/Week(L:T:P:S)	3:0:0:1	SEEMarks	50
TotalHoursofPedagogy	40	TotalMarks	100
Credits	3	ExamHours	3

Courseobjectives:

- ImpartknowledgeofMOStransistortheoryandCMOStechnologies
- Impartknowledgeonarchitecturalchoicesandperformance trade-offsinvolvedindesigningandrealizingthecircuitsin CMOStechnology
- Cultivatetheconceptsofsubsystemdesignprocesses
- DemonstratetheconceptsofCMOStesting

Teaching-LearningProcess(GeneralInstructions)

Thesamplestrategies,whichtheteachercanusetoacceleratetheattainmentofthevariouscourseoutcomesare listedin thefollowing:

1. Lecturemethod(L)doesnotmeanonlythetraditionallecturemethod,butadifferenttypeofteachin gmethodmaybeadopted todevelop theoutcomes.
2. ShowVideo/animationfilmstoexplainthefunctioningofvarioustechniques.
3. Encouragecollaborative(Group)Learningintheclass
4. AskatleastthreeHOTS(Higher-orderThinking)questionsintheclass,whichpromotescriticalthinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinkingskillssuchastheabilitytoevaluate,generalize,andanalyzeinformationratherthansimplyreca llit.
6. Showthedifferentwaystosolvethesameproblemandencouragethestudentstocomeupwiththeirow ncreative ways to solvethem.
7. Discusshoweveryconceptcanbeappliedtotherealworld-andwhenthat'spossible,ithelpsimprovethe students'understanding.
8. IncorporateprogrammingexamplesgivenunderActivitybasedlearning.

Module-1

Introduction:ABrief History,MOS Transistors, MOSTransistor Theory,IdealI-V Characteristics,Non-idealI-VEffects,DCTransferCharacteristics (1.1,1.3,2.1,2.2, 2.4,2.5ofTEXT2).
Fabrication:nMOSFabrication,CMOSFabrication[P-wellprocess,N-wellprocess,Twintubprocess],BiCMOSTechnology (1.7,1.8,1.10of TEXT1).

Teaching-LearningProcess	Chalkandtalkmethod,YouTubevideos,Powerpointpresentation **RBTLevel:**L1,L2

Module-2

MOSandBiCMOSCircuitDesignProcesses:MOSLayers,StickDiagrams,DesignRulesandLayout.
BasicCircuitConcepts: SheetResistance,AreaCapacitancesofLayers,StandardUnitofCapacitance, SomeAreaCapacitanceCalculations,DelayUnit,InverterDelays,DrivingLargeCapacitiveLoads(3.1to3.3,4.1,4.3to4.8ofTEXT1).

Teaching-LearningProcess	Chalkandtalkmethod/Powerpointpresentation **RBTLevel:**L1,L2, L3

Module-3	
ScalingofMOSCircuits:ScalingModels&ScalingFactorsforDeviceParameters **Subsystem Design Processes**: Some General considerations, An illustration of Design Processes,**Illustration of the Design Processes**: Regularity, Design of an ALU Subsystem, The Manchester Carry-chainandAdderEnhancementTechniques (5.1,5.2, 7.1,7.2,8.2,8.3, 8.4.1,8.4.2 ofTEXT1).	
Teaching-LearningProcess	Chalkandtalkmethod,YouTubevideos,Powerpointpresentation **RBTLevel:**L1,L2, L3
Module-4	
SubsystemDesign:Some ArchitecturalIssues,SwitchLogic,Gate(restoring)Logic,ParityGenerators,Multiplexers, The ProgrammableLogicArray(PLA) (6.1to6.3,6.4.1,6.4.3,6.4.6 ofTEXT1). **FPGABasedSystems**:Introduction,Basicconcepts,DigitaldesignandFPGAs,FPGAbasedSystemdesign,FPGA architecture, Physical designfor FPGAs(1.1to1.4,3.2,4.8ofTEXT3).	
Teaching-LearningProcess	Chalkandtalkmethod,YouTubevideos,Powerpointpresentation **RBTLevel:**L1,L2, L3
Module-5	
Memory,RegistersandAspectsofsystemTiming:SystemTimingConsiderations,SomecommonlyusedStorage/Memoryelements(9.1,9.2ofTEXT1). **Testing and Verification**: Introduction, Logic Verification, Logic Verification Principles,ManufacturingTestPrinciples,Designfortestability (12.1,12.1.1, 12.3, 12.5,12.6ofTEXT2).	
Teaching-LearningProcess	Chalkandtalkmethod/Powerpointpresentation **RBTLevel:**L1,L2, L3

Courseoutcome(CourseSkillSet)

Attheendofthecoursethestudentwillbeableto:

1. DemonstrateunderstandingofMOStransistortheory,CMOSfabricationflowandtechnologyscaling.
2. Drawthebasicgatesusingthestickandlayoutdiagramswiththeknowledgeofphysicaldesignaspects.
3. InterpretMemoryelementsalongwithtimingconsiderations
4. DemonstrateknowledgeofFPGAbasedsystemdesign
5. InterprettestingandtestabilityissuesinVLSIDesign
6. AnalyzeCMOSsubsystemsandarchitecturalissueswiththedesignconstraints.

AssessmentDetails(bothCIEandSEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%.The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50). A studentshall be deemed to have satisfied the academic requirements and earned the credits allotted to eachsubject/ course if the student secures not less than 35% (18 Marks out of50) in the semester-endexamination (SEE), and a minimum of 40% (40 marks out of 100) in the sum total of the CIE (ContinuousInternalEvaluation)andSEE(Semester End Examination)taken together.

ContinuousInternalEvaluation:

ThreeUnitTestseachof **20Marks(duration01hour**)

1. Firsttestattheendof5thweekofthesemester
2. Secondtestattheendofthe10thweekofthesemester
3. Third test at the end of the 15thweek of the

semesterTwo assignmentseachof**10 Marks**

4. Firstassignmentattheendof4thweek ofthesemester
5. Secondassignmentat theendof9thweekofthesemester

Group discussion/Seminar/quiz any one of three suitably planned to attain the COs and POs for **20Marks** (**duration01 hours**)

6. Attheendofthe13th weekofthesemester

Thesumofthreetests,twoassignments,andquiz/seminar/groupdiscussionwillbeoutof100marksandwillbe **scaled downto50marks**

(tohavelessstressedCIE,theportionofthesyllabusshouldnotbecommon/repeatedforanyofthemethodsofth eCIE.Eachmethod ofCIEshouldhaveadifferentsyllabusportionof thecourse).

CIEmethods/questionpaperisdesignedtoattainthedifferentlevelsofBloom'staxonomyaspertheoutco me defined for thecourse.

SemesterEndExamination:

TheorySEEwillbeconductedbyUniversityasperthescheduledtimetable,withcommonquestionpapersforthes ubject(**duration 03 hours)**

1. Thequestionpaperwillhavetenquestions.Eachquestionissetfor20marks.
2. Therewillbe2questionsfromeachmodule.Eachofthetwoquestionsunderamodule(withamaximum of3sub-questions),**shouldhaveamixoftopics**underthat module.

The students have to answer 5 full questions, selecting one full question from each module.Marks scoredoutof100shallbe reducedproportionallyto50marks

SuggestedLearningResources:

TextBooks:

1. "BasicVLSIDesign"- DouglasAPucknell&KamranEshraghian,PHI,3rd Edition.
2. "CMOSVLSIDesign-ACircuitsandSystemsPerspective",NeilHEWeste,DavidHarris,AyanBanerjee,3rd Edition,PearsonEducation.
3. "FPGABasedSystemDesign",WayneWolf,PearsonEducation,2004,TechnologyandEngineering.

WeblinksandVideoLectures(e-Resources)

- https://nptel.ac.in/courses/117101058
- https://nptel.ac.in/courses/117106093
- https://youtu.be/9SnR3M3CIm4
- https://nptel.ac.in/courses/108/107/108107129/

ActivityBasedLearning(SuggestedActivitiesinClass)/PracticalBasedlearning

Wherevernecessary**Cadence/Synopsis/MentaGraphicstools**mustbeused.

1.WriteVerilogCodeforthefollowingcircuitsandtheirTestBenchforverification,observethewaveform and synthesize the code with technological library with given Constraints*. Do the initialtimingverification withgatelevel simulation.

i. Aninverter
ii. ABuffer
iii. TransmissionGate
iv. Basic/universalgates
v. Flipflop -RS,D, JK,MS, T
vi. Serial&Paralleladder
vii. 4-bitcounter[SynchronousandAsynchronouscounter]

2.Designanop-ampwithgivenspecification*usinggivendifferentialamplifierCommonsourceandCommonDrainamplifieri nlibrary**and completingthedesignflowmentionedbelow:

a. Drawtheschematicandverifythefollowing
   i) DCAnalysis
   ii) ACAnalysis
   iii) TransientAnalysis
b. DrawtheLayout andverifytheDRC,ERC
c. CheckforLVS
d. ExtractRCandbackannotatethesameandverifythe Design.

03.10.2022

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
B.E: Electronics and Communication Engineering
NEP, Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
(Effective from the academic year 2022-2023)

V Semester

NOTE: This Laboratory can be conducted using Industry standard EDA tool like Cadence , Synopsis or any equilent VLSI tool.

VLSI Design and Testing LAB			
Course Code	**BECL606**	CIE Marks	50
Teaching Hours/Week (L: T: P: S)	0:0:2:0	SEE Marks	50
Credits	1	Exam Hours	3

Course objectives:

This laboratory course enables students to

- Design, model, simulate and verify digital circuits.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints andevaluating the synthesis reports to obtain optimum gate level netlist.
- Perform RTL-GDSII flow and understand the ASIC Design flow.

Sl.No.	Experiments
1	Design a 4-Bit Adder • Write a Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and generate the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
2	4-Bit Shift and add Multiplier • Write Verilog Code • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report generated identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required
3	32-Bit ALU Supporting 4-Logical and 4-Arithmetic operations, using case and if statement for ALUBehavioral Modeling • Write Verilog description • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist • Identify Critical path
4	Flip-Flops (D,SR and JK) • Write the Verilog description • Verify the Functionality using Test-bench • Synthesize the design by setting proper constraints and obtain the gate level netlist. From the report gate level netlist identify Critical path, Maximum delay, Total number of cells, Power requirement and Total area required. • Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
5	Four bit Synchronous MOD-N counter with Asynchronous reset • Write Verilog Code • Verify functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist Identify Critical path

	• Verify the functionality using Gate level netlist and compare the results at RTL and gate level netlist.
6	a) Construct the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: i. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and the time period of 20ns and plot the input voltage and output voltage of designed inverter? ii. From the simulation result compute tpHL, tpLH and td for all three geometrical settings of width? iii. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre layout simulations and compare the results.
7	Capture the schematic of 2-input CMOS NOR gate having similar delay as that of CMOS inverter computed in experiment above. Verify the functionality of NOR gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increasethe drive strength to 2X and 4X and tabulate the results.

8	Construct the schematic of the Boolean Expression $Y = AB+CD+E$ using CMOS Logic. Verify the functionality of the expression find out the delay td for some combination of input vectors. Tabulate the results.
9	a) Construct the schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measure the Unit Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB. b) Draw Layout of common source amplifier, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.
10	a) Construct the schematic of two-stage operational amplifier and measure the following: i. Unity gain Bandwidth ii. dB Bandwidth iii. Gain Margin and phase margin with and without coupling capacitance iv. Use the op-amp in the inverting and non-inverting configuration and verify its functionality. v. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in part a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations and perform the comparative analysis.
	Demonstration Experiments (For CIE)

11	UART • Write Verilog description • Verify the Functionality using Test-bench • Synthesize the design targeting suitable library and by setting area and timing constraints • Tabulate the Area, Power and Delay for the Synthesized netlist, Identify Critical path

12	Design and characterize 6T binary SRAM cell and measure the following: • Read Time, Write Time, SNM, Power • Draw Layout of 6T SRAM, use optimum layout methods. Verify for DRC & LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record theobservations.

Course outcomes (Course Skill Set):

On the completion of this laboratory course, the students will be able to:

1. Design and simulate combinational and sequential digital circuits using Verilog HDL.
2. Understand the synthesis process of digital circuits using EDA tool.
3. Perform ASIC design flow and understand the process of synthesis, synthesis constraints andevaluating the synthesis reports to obtain optimum gate level netlist.
4. Design and simulate basic CMOS circuits like inverter, NOR gate and any Boolean expression .
5. Perform RTL_GDSII flow and understand the stages in ASIC design.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks). A student shallbe deemed to have satisfied the academic requirements and earned the credits allotted to each course. The student has to secure not less than 35% (18 Marks out of 50) in the semester-end examination (SEE).

Continuous Internal Evaluation (CIE):

CIE marks for the practical course is **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment to be evaluated for conduction with observation sheet and record write-up. Rubricsfor the evaluation of the journal/write-up for hardware/software experiments designed by the faculty who is handling the laboratory session and is made known to students at the beginning of thepractical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up willbe evaluated for 10 marks.
- Total marks scored by the students are scaled downed to 30 marks (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct 02 tests for 100 marks, the first test shall be conducted after the 8^{th} weekof the semester and the second test shall be conducted after the 14^{th} week of the semester.
- In each test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.Rubrics suggested in Annexure-II of Regulation book
- The average of 02 tests is scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and average marks of two tests is the total CIE marks scored by the student.

03.10.2022

Semester End Evaluation (SEE):

SEE marks for the practical course is 50 Marks.

SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the University

All laboratory experiments are to be included for practical examination.
(Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be

decided jointly by examiners.
Students can pick one question (experiment) from the questions lot prepared by the internal /external examiners jointly.
Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.
General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners).
Change of experiment is allowed only once and 15% Marks allotted to the procedure part to be madezero.
The duration of SEE is 03 hours.
Rubrics suggested in Annexure-II of Regulation book

03.10.2022

FPGA Based System design Lab Using Verilog		Semester	VI
Course Code	**BEC657A**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course objectives:

This laboratory course enables students to

- Understand FPGA Design flow for VLSI Chip Design
- Understand the concept of Design and implementation of Advanced Digital System Design
- Learning the Implementation of advanced digital circuits on FPGA boards

	Verilog Program can be compile using any compiler, Verifying the functionality using suitable simulator. Down load the programs on FPGA boards and Verify the Functionality
1	Write a Verilog description for the following combinational logic, Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. Structural modelling of Full adder using two half adders and or Gate b. BCD to Excess-3 code converter
2	Write a Verilog description for the following Sequential Circuits,Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. Mod-N counter b. Random sequence counter
3	Write a Verilog description for the following Sequential Circuits, Verify the design using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. SISO and PISO shift register b. Ring counter
4	Write a Verilog description for the following Digital Circuits, Verify the functionality usingVerilog test bench and perform the synthesis by downloading the design on to FPGA device. a.4-Bit Ripple Carry Adder b. 4-Bit Linear Feedback shift register
5	Write a Verilog description for the following Digital Circuits, Verify the functionality using Verilog test bench and perform the synthesis by downloading the design on to FPGA device. a. 4-bitArray Multiplication b. 4-bit Booth Multiplication

6	Write a Verilog description to design a clock divider circuit that generates 1/2, 1/3rdand 1/4thclock from a given input clock. Port the design to FPGA and validate the functionality using output device.
7	Interface a Stepper motor to FPGA andWrite a Verilog description to controlStepper motor rotation.
8	Interface a DAC to FPGA and Write a Verilog descriptionto generate Squre wave of frequency F KHz. Modify the code to down sample the frequency to F/2 KHz. Display the original and Down sampled signals by connecting them to an output device.
9	Write a Verilog descriptionto convert an analog input of a sensor to digital form and to display the same on a suitable display like set of simple LEDs like 7-Segment display digits.

Course outcomes:

- Familiarize with the EDA tool to write HDL programs to understand simulation and synthesis of digital design.
- Design, Simulation and Synthesis of Combinational circuits using EDA tool
- Design, Simulation and Synthesis of Sequential Circuits using EDA tool
- Interfacing DAC to FPGA device to generate different waveforms using Verilog HDL.
- Interfacing Stepper motor to FPGA device to count the number of rotations of a stepper motor.

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Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1) SamirPalnitkar, "Verilog HDL : A guide to digital design and synthesis", Pearson Education, II Edition.

2) Donald E Thomas, Philip R Moorby, "The Verilog hardware description Language", Springer Science Business Media , LLC, 5th Edition

3) Michael D. Ciletti, "Advanced digital design with the Verilog HDL", Pearson (PHI),II Edition

4) Padmanabhan, Tripura Sunadri, "Design through Verilog HDL", Wiley, 2016.

5) Verilog HDL user manual

System Modelling using Simulink		Semester	5
Course Code	**BEC657B**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Total SEE+CIE	100
		Exam Hours	2 Hours
Examination type (SEE)	**Practical**		

Course objectives:

- Understand the basics of MATLAB Simulink used for engineering applications
- Simulation of the trigonometric functions and display of signals.
- Implementations of analog and digital systems using Simulink.
- Implement digital logic circuits using Simulink and display the output.
- Simulation of the analog and digital communication systems using Simulink.

Sl.NO	Experiments
1	a) Generate the following signals using Simulink and display these signals on a single scope with separate inputs. i) sinusoidal signal, ii)square signal, iii) sawtooth signal, and iv) random signal b) Perform the following operations using simulink and display the output. i) y(t) = sin2t, ii) y(t) = $\frac{d(sin2t)}{dt}$, iii)y(t) = $\int sin2t$
2	Solve the second order differential equations shown below using Simulink and display the output. i) $\frac{d^2y}{dt^2} + 2\frac{dy}{dt} + 5y = 1$ ii) $\frac{d^2y}{dt^2} + 3\frac{dy}{dt} + 4y = 5\cos 2t$
3	Design and realize the second order low pass and high pass RC filters using Simulink.
4	Design a BCD adder and use Simulink to simulate and verify its operation.
5	Design and Simulate the following using Simulink and verify its operation. a) 3–bit Up / Down Counter, b) 4–bit Ring Counter
6	Design and simulate the 4x1 Multiplexer and 1x4 Demultiplexer using Simulink
7	Find the step response of the following system functions given below, using Simulink. i) Continuous transfer function H(s) = $\frac{5(s+2)}{s(2s^2+4s+3)}$ ii) Discrete transfer function H(z) = $\frac{z^2-1.2z+1}{z^3-1.3z^2+z-0.2}$
8	Realize the FIR filter given by the impulse response h(n) = {0.08, 0.21,0.54, 0.86, 1, 0.86, 0.54, 0.21 0.08) using Simulink. Obtain the frequency response characteristics.

9	Simulate the Amplitude Modulation and Demodulation using Simulink. Display the output signal and its spectrum.
10	Simulate the modulation & demodulation of a random binary data stream using QPSK using Simulink. Display the output signal and its spectrum.

Course outcomes (Course Skill Set):

At the end of the course the student will be able to:

- Create Simulink models to perform analog and digital computations.
- Implement the Combinational Digital circuits and Sequential Digital Circuit models using Simulink.
- Implement analog and digital systems using the transfer functions in s-domain and z-domain respectively.
- Demonstration of analog and digital communication modulation and demodulation using Simulink.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment is to be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- Record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- Total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage to be given for neatness and submission of record/write-up on time.
- Department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted by the two examiners. One from the same institute as an internal examiner and another from a different institute as an external examiner, appointed by the university.**
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted between the schedule mentioned in the academic calendar of the University.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be

strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.

- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

1. Steven T. Karris, "Introduction to Simulink® with Engineering Applications", Orchard Publications, 2011, ISBN : 978-1934404218
2. Devendra K. Chaturvedi, "Modeling and Simulation of Systems Using MATLAB and Simulink", CRC Press Taylor & Francis Group, 2010, ISBN 9780815351382

IoT (Internet of Things) Lab		Semester	6
Course Code	BEC657C	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course Objectives:

This course will enable students to

- To impart necessary and practical knowledge of components of the Internet of Things
- To develop skills required to build real-life IoT-based projects.

Sl.No.	Experiments
1(i)	To interface LED/Buzzer with Arduino /Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds.
1(ii)	To interface the Push button/Digital sensor (IR/LDR) with Arduino /Raspberry Pi and write a program to 'turn ON' LED when a push button is pressed or at sensor detection.
2 (i)	To interface the DHT11 sensor with Arduino /Raspberry Pi and write a program to print temperature and humidity readings.
2(ii)	To interface OLED with Arduino /Raspberry Pi and write a program to print its temperature and humidity readings.
3	To interface the motor using a relay with Arduino /Raspberry Pi and write a program to 'turn ON' the motor when a push button is pressed.
4(i)	Write an Arduino/Raspberry Pi program to interface the Soil Moisture Sensor.
4(ii)	Write an Arduino/Raspberry Pi program to interface the LDR/Photo Sensor.
5	Write a program to interface an Ultrasonic Sensor with Arduino /Raspberry Pi.
6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to _thingspeak cloud.
7	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from _thingspeak _cloud.
8	Write a program to interface LED using Telegram App.
9	Write a program on Arduino/Raspberry Pi to publish temperature data to the MQTT broker.
10	Write a program to create a UDP server on Arduino/Raspberry Pi and respond with humidity data to the UDP client when requested.
11	Write a program to create a TCP server on Arduino /Raspberry Pi and respond with humidity data to the TCP client when requested.
12	Write a program on Arduino / Raspberry Pi to subscribe to the MQTT broker for temperature data and print it.

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Explain the Internet of Things and its hardware and software components.
- Interface I/O devices, sensors & communication modules.
- Remotely monitor data and control devices.

- Develop real-life IoT-based projects.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%, Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

- Vijay Madisetti, Arshdeep Bahga, Internet of Things. "A Hands-on Approach", University Press
- Dr. SRN Reddy, Rachit Thukral, and Manasi Mishra, "Introduction to Internet of Things: A Practical Approach", ETI Labs
- Pethuru Raj and Anupama C Raman, "The Internet of Things: Enabling Technologies, Platforms, and Use Cases", CRC Press
- Jeeva Jose, "Internet of Things", Khanna Publishing House, Delhi
- Adrian McEwen, "Designing the Internet of Things", Wiley
- Raj Kamal, "Internet of Things: Architecture and Design", McGraw Hill

Python Programming for Machine Learning Applications		Semester	**6**
Course Code	BEC657D	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	0:0:2:0	SEE Marks	50
Credits	01	Exam Hours	3
Examination type (SEE)	Practical		

Course Objectives:

This course will enable students to

- To impart necessary and practical knowledge Machine Learning Algorithms
- To develop skills required to build real-life ML Algorithm projects.

Sl.No.	Experiments
1	Solve the Tic-Tac-Toe problem using the Depth First Search technique.
2	Show that the 8-puzzle states are divided into two disjoint sets, such that any state is reachable from any other state in the same set, while no state is reachable from any state in the other set.
3	To represent and evaluate different scenarios using predicate logic and knowledge rules.
4	To apply the Find-S and Candidate Elimination algorithms to a concept learning task and compare their inductive biases and outputs.
5	To construct a decision tree using the ID3 algorithm on a simple classification dataset
6	To assess how the ID3 algorithm performs on datasets with varying characteristics and complexity, examining overfitting, underfitting, and decision tree depth.
7	To examine different types of machine learning approaches (Supervised, Unsupervised, Semi-supervised, and Reinforcement Learning) by setting up a basic classification problem and exploring how each type applies differently
8	To understand how Find-S and Candidate Elimination algorithms search through the hypothesis space in concept learning tasks, and to observe the role of inductive bias in shaping the learned concept.
9	To go through all stages of a real-life machine learning project, from data collection to model fine-tuning, using a regression dataset like the "California Housing Prices."
10	To perform binary and multiclass classification on the MNIST dataset, analyze performance metrics, and perform error analysis.
11	**Demo experiments**
12	Demo experiments

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

- Apply machine learning algorithms to real life problems.
- Able to make use of different machine learning approaches.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). A student shall be deemed to have satisfied the academic requirements and earned the credits allotted to each subject/ course if the student secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Continuous Internal Evaluation (CIE):

CIE marks for the practical course are **50 Marks**.

The split-up of CIE marks for record/ journal and test are in the ratio **60:40**.

- Each experiment will be evaluated for conduction with an observation sheet and record write-up. Rubrics for the evaluation of the journal/write-up for hardware/software experiments are designed by the faculty who is handling the laboratory session and are made known to students at the beginning of the practical session.
- The record should contain all the specified experiments in the syllabus and each experiment write-up will be evaluated for 10 marks.
- The total marks scored by the students are scaled down to **30 marks** (60% of maximum marks).
- Weightage is to be given for neatness and submission of record/write-up on time.
- The department shall conduct a test of 100 marks after the completion of all the experiments listed in the syllabus.
- In a test, test write-up, conduction of experiment, acceptable result, and procedural knowledge will carry a weightage of 60% and the rest 40% for viva-voce.
- The suitable rubrics can be designed to evaluate each student's performance and learning ability.
- The marks scored shall be scaled down to **20 marks** (40% of the maximum marks).

The Sum of scaled-down marks scored in the report write-up/journal and marks of a test is the total CIE marks scored by the student.

Semester End Evaluation (SEE):

- SEE marks for the practical course are 50 Marks.
- **SEE shall be conducted jointly by the two examiners of the same institute, examiners are appointed by the Head of the Institute**.
- The examination schedule and names of examiners are informed to the university before the conduction of the examination. These practical examinations are to be conducted within the schedule mentioned in the university's academic calendar.
- All laboratory experiments are to be included for practical examination.
- (Rubrics) Breakup of marks and the instructions printed on the cover page of the answer script to be strictly adhered to by the examiners. **OR** based on the course requirement evaluation rubrics shall be decided jointly by examiners.
- Students can pick one question (experiment) from the questions lot prepared by the examiners jointly.
- Evaluation of test write-up/ conduction procedure and result/viva will be conducted jointly by examiners.

General rubrics suggested for SEE are mentioned here, writeup-20%, Conduction procedure and result in -60%,

Viva-voce 20% of maximum marks. SEE for practical shall be evaluated for 100 marks and scored marks shall be scaled down to 50 marks (however, based on course type, rubrics shall be decided by the examiners)

Change of experiment is allowed only once and 15% of Marks allotted to the procedure part are to be made zero.

The minimum duration of SEE is 02 hours

Suggested Learning Resources:

Text Book:

1. Stuart J. Russell and Peter Norvig , Artificial Intelligence, 3rd Edition, Pearson,2015

2. Elaine Rich, Kevin Knight, Artificial Intelligence, 3rd Edition,Tata McGraw Hill,2013.

3. Tom M. Mitchell, Machine Learning, McGraw-Hill Education, 2013

4. AurelienGeron, Hands-on Machine Learning with Scikit-Learn &Tensor Flow , O'Reilly, Shroff Publishers and Distributors Pvt. Ltd 2019.